Nanowatt Clock and Data Recovery for Ultra-Low Power Wake-Up Receivers

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Abstract

This paper presents the design of a data-startable baseband logic for wake-up receivers (WuRxs) enabling nodes to receive infinite bits in addition to a codeword. The proposed integrated circuit includes a control logic with addressing capabilities and a clock and data recovery (CDR) block based on a Gated Oscillator (GO). At each data transition the phase misalignment between received data and clock is compensated in a highly energy-efficient way thus allowing to correctly receive infinite bits. The difference between the Gated Oscillator free-running frequency and the bit-rate limits only the maximum number of equal consecutive bits that can be received. A design is presented in STMicroelectronics 90-nm BCD technology 1.2-V supply. Baseband logic has been supplied with 0.6 V to reduce overall consumption. The overall power consumption is 4.78 nW during the rest state and 9 pJ/bit at 1-kbps data rate. The CDR circuit alone consumes 0.162 nW during the rest state and 4.23 nW in active state that results in 4.23 pJ/bit at 1-kbps data rate.

Keywords—IoT applications, clock and data recovery, gated oscillator, nanowatt wake-up radio, ultra-low power data receiver.

1 Introduction

Energy efficiency is a crucial metric for all battery-powered devices such as Wireless Sensor Networks (WSNs). In a typical WSN, the most power-hungry subsystem of the wireless sensor node is the communication one. On the other hand, the nodes spend the majority of their time without the need to send a message. To increase the energy efficiency, the nodes tend to reduce activity of the radio transceiver. Among other technologies, the employment of Wake-Up receivers (WuRx) drastically reduces the power consumption of the sensor nodes keeping them in asleep-yet-awake states [1][2]. A WuRx is an always-on ultra-low-power receiver, which typically employs On-Off-Keying (OOK) messages, used to wake-up the node if a communication request is detected. Fig. 1 shows a typical WuRx architecture which is composed of two subsystems: an analog front-end (AFE) and a baseband logic.

In particular, the AFE is an OOK demodulator which converts the RF input signal into a stream of bits. The baseband logic generates the wake-up signal upon reception of the correct codeword. The performances of the WuRx are conventionally evaluated on four metrics: 1) sensitivity, 2) data rate, 3) power consumption and 4) wake-up latency.

State of the art WuRxs employ clocked or clockless analog front-ends while baseband logic typically uses oversampling or digital control techniques to overcome phase misalignment between the received data and the internal clock [2-5]. While AFE can detect infinite bits, baseband architectures can process codewords with a maximum length ranging from 8 to 32 bits, thus a frequency error of a few percent between clock and data is tolerable, with no need of power-hungry PLL-like circuits or crystal oscillators for precise frequency control. In [6] it is shown how it is possible to use the WuRx to receive a 40-bit sequence using a data-locked startable oscillator. Recently in [7] the issue to receive longer sequences of data in addition to codeword, at the cost of microwatt power consumption, was investigated.

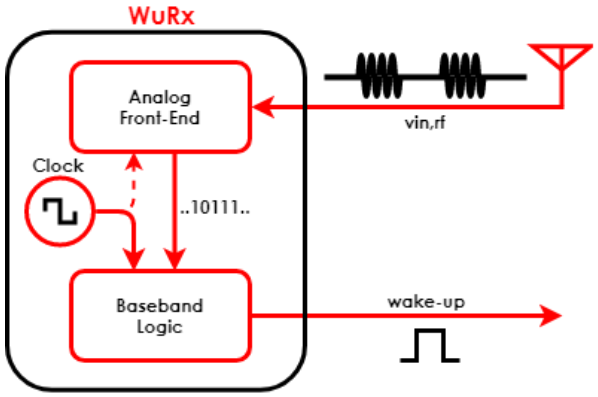

Fig. 1. Typical WuRx architecture. AFE may use or not an internal clock.

In this paper, we introduce the design of a WuRx data-startable baseband logic enabling long data transmission applications (i.e. several tens or hundreds of bits), while keeping the ultra-low-power capability of state-of-the-art WuRxs. The proposed baseband logic consists of: i) a clock and data recovery (CDR) circuit based on the Gated Oscillator (GO) architecture [8][9], which enables to receive infinite bits by guaranteeing both phase and frequency alignment between the received data and the clock, and ii) a control logic with addressing capabilities (CL).

The functionalities of the proposed circuit are evaluated with the AFE presented in [10] that achieves -54-dBm sensitivity with a power consumption of 13.2 nW for a 1-kbps OOK signal with an 868 MHz carrier.

From the system point of view, this augmented capability of the WuRx would enable it to operate as an ultra-low-power secondary receiver, allowing to reduce the power consumption of the entire WSN. Two types of wake-up interrupts would

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become available: i) standard wake-up to wake-up the entire node and perform a communication through the main radio and ii) wake-up with storage/processing that enables the reception of data that can be stored in memory and/or processed without the need to wake-up the main radio. As a possible application, in case the WuRx is installed in actuator and sensor nodes, this feature allows receiving packets for parameter configuration and special instructions and commands. This would avoid the main radio activation for data transmission and synchronization with the gateway. Moreover, in case the WuRx is used in a static WSN sink node, this capability would allow to receive and store the data coming from other sensor nodes without activating the main radio before sending all the gathered data at once. Receiving not-limited sequence of bits with the WuRx enables the possibility to receive also encrypted data to increase the security of the transmission [11]. This paper is organized as follows: in section II a WuRx for long transmissions applications is presented, in section III the circuit implementation of the proposed architecture is described, in section IV simulation results are shown and in section V conclusions are drawn.

2 A WuRx Architecture for Long Transmissions Applications

A. Clockless analog front-end

In this paragraph, we discuss the features that the AFE must possess in order to accommodate the proposed baseband logic.

With reference to Fig. 1, AFEs can be classified either as clocked or clockless, regarding their eventual need of an internal oscillator. In both solutions, the AFE is always-on since it has to detect the presence of an incoming message. Clocked AFE solutions, as reported in [2-5], employ an envelope detector (ED) followed by a latched comparator to generate binary signals. In these solutions, the always-on clock is used also by the baseband logic. Recently, clockless AFEs have been presented [6][10]: they allow a reduction of the overall WuRx power consumption since an always-on oscillator is not required, but lose the benefit of the positive feedback of latched comparators.

When clockless AFE architectures are used the WuRx operates in two phases [6]:

- phase 1: the baseband logic is off while the AFE is the only active section.
- phase 2: upon recognition of the first transition of an incoming message, the second phase starts and the baseband logic is turned on from the rest state to process the incoming data. After receiving the whole stream, the system is set back to phase 1.

The baseband logic proposed in the next subsection requires that a clockless AFE is adopted. In particular, the one described in [10] is used to verify the functionalities of the proposed solution.

B. Proposed baseband logic block

In state-of-the-art WuRx, oversampling techniques are typically used in order to overcome phase misalignment between received data and internal clock. These architectures employ either relaxation or crystal oscillators. Neither solution is completely satisfactory for long transmissions, which are the object of this paper. Indeed, relaxation oscillators offer ultra-low power consumption (few nanowatts). Their frequency precision under process and temperature variations is limited to few percent. On the other side, crystal oscillators offer optimum frequency stability but at the cost of higher power consumption (tens of nanowatts). For example, the WuRx reported in [3] uses a relaxation oscillator that consumes 1.1 nW at 1.2 kHz with a frequency accuracy of 5%, which allows sampling a 16-bit code, while the crystal oscillator in [4] consumes 40 nW at 50 kHz. The baseband logic proposed in this work is shown in Fig. 2-A: it is composed of a GO-CDR block and a CL. The GO-CDR eliminates the effects of phase/frequency misalignments without using power-hungry oscillators and is similar to the ones proposed in [12][13], which however targeted very different applications with data rate ranging between 200-350 kbps and power consumption between 5 µW and 6 µW. We show here that similar GO-CDR can be designed with nanowatt power as required by the present application.

B.1. Gated-oscillator based CDR

The CDR circuit in Fig. 2-A must detect the transitions in the received data and generate a clock signal with a frequency equal to the data-rate. The phase/frequency relationship between the received data and the generated clock in the ideal case is shown in Fig. 2-B. It is shown that the positive clock edge occurs at the center of each bit-time, which is the ideal sampling time.

A PLL implementation of the CDR is ruled out because it requires high R-C values and hence long preamble times to keep power consumption in the nanowatt range.

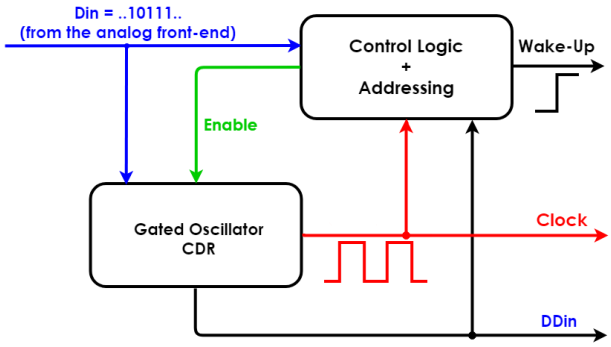

Fig. 2-A. Baseband logic. Din is the input data coming from the AFE, DDin is the delayed version of Din, Enable is used to turn on/off the CDR circuit.

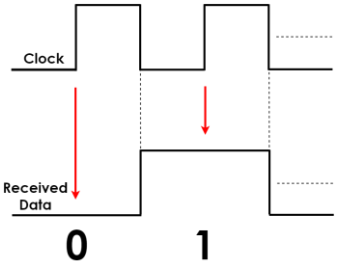

Fig. 2-B. Phase and frequency alignment between the received data and the clock signal generated by the CDR.

In this paper, we propose the GO-CDR [8][9] shown in Fig. 3. It is composed of three main blocks: a) a Delay block (DB),

b) an Edge Detector (EXNOR) and c) the Gated Oscillator, plus an additional biasing block. The sampling block is not part of the CDR but is included in Fig. 3 to highlight that DDin instead of Din is sampled. DDin generated by DB is a delayed replica of Din, τ_d being the time delay. The edge detector is implemented by a simple EXNOR. Its output signal Gate is normally 1, with a 0 pulse of width τ_d for each transition of Din, as illustrated in Fig. 4. The behavior of the GO is the following:

- when Gate = 1 the oscillator is in free-running mode with frequency $f_{ck} = 1/T_{ck}$,
- when Gate = 0 the oscillator is blocked and reset to a predefined state with Clock = 0 steadily.

The operation of the entire CDR circuit is described by the waveforms in Fig. 4, where T_b is the bit time and $T_b = T_{ck}$ is assumed for drawing purpose only.

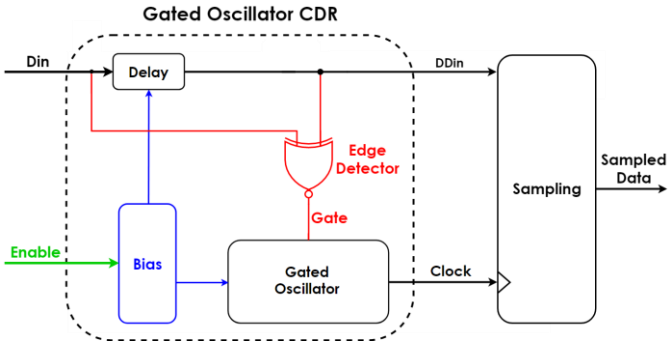

Fig. 3. Gated oscillator CDR circuit.

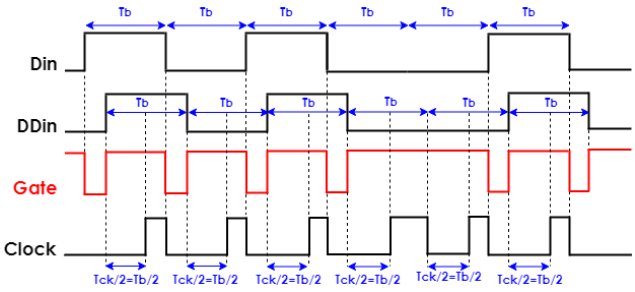

Fig. 4. Gated oscillator CDR circuit behavior.

At each Din transition, a zero-pulse of Gate is generated, Clock is reset and any phase error accumulated up to that time is erased. When Gate goes back to 1, the GO enters free-running mode again, the first Clock positive edge ideally being generated after $T_{ck}/2$. Therefore, as long as Gate remains at 1, DDin is sampled with frequency f_{ck}. If $T_b \neq T_{ck}$ a phase error will start to accumulate again, which however will be suppressed at the first occurrence of a data transition. Therefore, the constraint is on the maximum number of equal consecutive bits (NECB), not on the total number of transmitted bits.

The following conditions must be satisfied for the correct operation of the CDR circuit. To have a non-null duration of the clock high phase,

$$\frac{T_b}{2} - \tau_d > 0 \qquad (1)$$

must be guaranteed, which sets an upper value for τ_d. On the other side, τ_d must be longer than the time ($\tau_{d,res}$) required to correctly reset the oscillator

$$\tau_d > \tau_{d,res} \qquad (2)$$

NECB can be calculated imposing that no bit is sampled twice (which could occur if $T_{ck} < T_b$) or not sampled at all (if $T_{ck} > T_b$). Defining $\alpha = |T_{ck} - T_b|/T_b$, a simplified analysis leads to the following conditions:

$$\frac{T_{ck}}{2} + nT_{ck} > nT_b \qquad \text{when } T_{ck} = T_b(1-\alpha) \qquad (3)$$

$$\frac{T_{ck}}{2} + nT_{ck} < (n+1)T_b \qquad \text{when } T_{ck} = T_b(1+\alpha) \qquad (4)$$

where $n = NECB$, resulting in:

$$NECB < \frac{1-\alpha}{2\alpha} \qquad (5)$$

For example, NECB = 2 if $\alpha = 0.2$ while NECB increases to 9 if $\alpha = 0.05$. In the limiting case, if a Manchester code is adopted, $\alpha \cong 0.2$ is acceptable, which is easily obtainable with many types of oscillators. On the contrary, if high values of NECB are required an additional frequency calibration circuit can be used. In practical implementations, as discussed in the next section, second order effects must also be taken into account, e.g. the differences between rise and fall delay times ($\tau_{d,rise}$ and $\tau_{d,fall}$, respectively) of DB and the oscillator start-up time (τ_{resp}) when Gate becomes 1. Moreover, the required accuracy must be guaranteed over Process, Voltage and Temperature (PVT) variations.

B2. Control logic

The CL in Fig. 2-A must detect the first edge of an incoming message and generate signal Enable that enters the WuRx into phase 2. Consequently, the GO is activated and the generated clock is used to correlate the incoming data with a predefined codeword. The CL generates the wake-up signal only when the correlation result is higher than a programmable threshold. It also decodes a start frame and an end frame delimiter indicating the start and the end of the data transmission, respectively. To avoid the CDR being worthless activated, the CL includes a programmable counter to generate a time-out signal that turns the whole baseband logic off in case the first detected edge is a spurious transition. When the transmission ends or the wake-up signal is generated, the baseband logic goes back to phase 1 as described in paragraph II-A.

C. WuRx to MCU interface

WuRx implementations currently proposed in the literature are designed to recognize a codeword or at most to process few tens of bits. In this paper, what we propose is a WuRx enabling the reception of infinite bits: in order to take fully advantage of this feature, an appropriate interface between WuRx and MCU (W2M) should also be designed, as shown in Fig. 5, with the capability to store and/or process the received data. The W2M, not included in the proposed design, can be implemented by using ultra-low-power dedicated logic that stores/processes DDin exploiting the clock generated by the proposed baseband logic. This unit, depending on the specific application, can also periodically configure the WuRx parameters (threshold, codeword, clock frequency, etc.). In particular, the W2M should be properly designed and programmed to distinguish, as

suggested in the Introduction, between standard wake-up and wake-up with storage/processing. In the first case, the WuRx wakes-up the MCU and the main radio keeping the W2M in sleep mode; in the second case, once woken-up, the W2M starts to store/process data while the MCU and the main radio are in sleep mode.

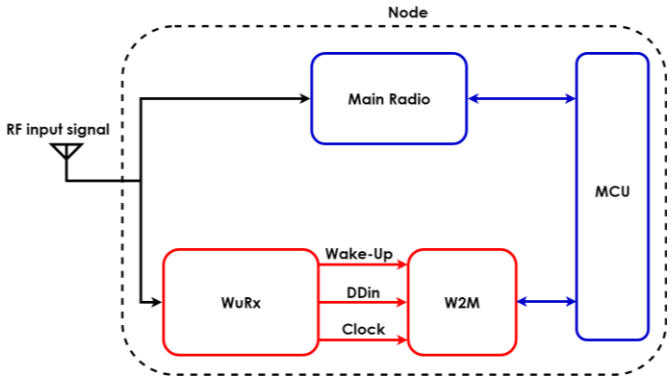

Fig. 5. WSN node with a WuRx including the baseband logic proposed in this paper and the WuRx to MCU interface (W2M).

3 Circuit Implementation

A. Gated Oscillator and Delay block

Fig. 6 shows the schematic diagram of the proposed GO. It is composed of a three-stages ring oscillator whose output (O3) is provided to an inverting/buffering stage to generate a squared clock signal (Clock). Each stage is composed of a current starved inverter (M1, M2, M3, M4), a capacitor C and two additional transistors (M5, M6) driven by control signal Gate (or !Gate) to force all the internal node voltages to predefined values when the oscillation is reset with Gate = 0. The oscillation frequency is given by $1/(2N\tau_p)$ where $N = 3$ is the number of stages and τ_p is the propagation delay of each inverter. The propagation delay τ_p varies with the current available to charge and discharge capacitance C, therefore it is controlled by the bias voltages of transistors M1 and M4 (*vbias_p*, *vbias_n*).

Fig. 7 shows the schematic diagram of the DB. It is composed of the same current starved inverter stage used for the design of the GO and is biased by the same control voltages *vbias_p*, *vbias_n*. Transistors M5 and M6 are always off and are included to force τ_d to be as close as possible to τ_p. The gate voltages of M5 and M6 are set to V_{dd} and *GND*, respectively. The inverting/buffering stage is used to generate a squared version (DDin) of the delayed data. The additional delay introduced by this buffering stage is negligible with respect to the one of the current starved stage τ_p and it can be assumed $\tau_d = \tau_p$. Therefore, $\tau_d = T_{ck}/6$ which guarantees that (1) is satisfied in any PVT condition for any reasonable value of α.

The bias circuit is shown in Fig. 8. It generates the control voltages *vbias_p* and *vbias_n* so as to have the charging/discharging currents of the GO equal to I_{bias}. By changing I_{bias} it is therefore possible to tune f_{ck} and τ_d.

The ratio between the currents flowing through M1 and M2 is set to 1:1 to prevent the circuit to operate in sub-nanoampere current region where the transistor models are not predictive. This choice implies that the CDR power consumption during phase 2 is mainly due to the bias circuit.

During phase 2, the power consumption contributions are $P_{bias} = 2V_{dd}I_{bias}$, $P_{DB} = \gamma C f_{ck} V_{dd}^2$ and $P_{GO} = 3C f_{ck} V_{dd}^2$ where γ is the switching activity depending on the input data pattern. P_{GO} is computed assuming the GO in free-running mode.

Signal Enable in Fig. 8 is generated by the CL and allow to put the GO and DB in a sleep state (phase 1), thus limiting power consumption in this phase only to transistor leakage currents.

B. Control logic

The control logic has been implemented starting from HDL behavioural description of the circuit. Implementation has been done targeting 1.2 V standard cell library following a standard implementationtion flow (synthesis and place&route). The resulting circuit complexity is of about 800 equivalent gates. To minimize the consumption, the target operating supply has been defined as 0.6 V hence the circuit has been verified through post-layout transistor-level simulations.

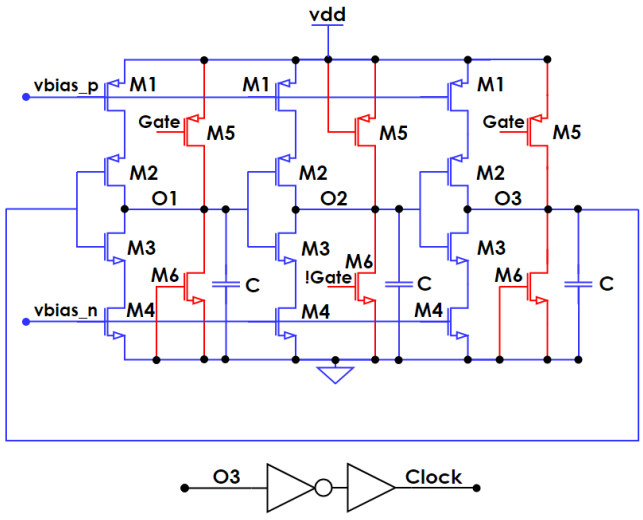

Fig. 6. Schematic of the proposed Gated Oscillator (GO).

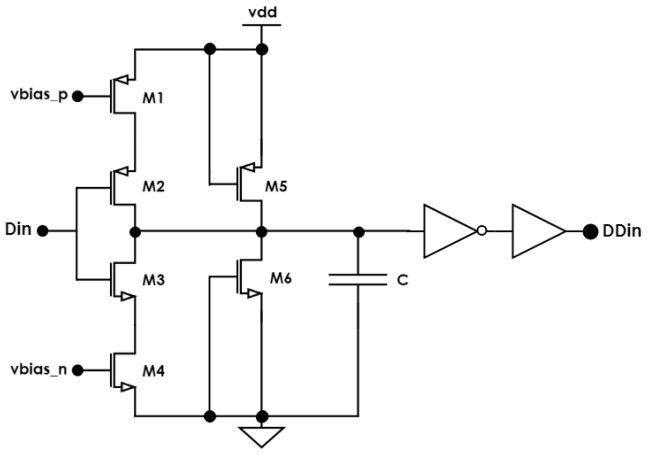

Figure 7. Schematic of the proposed Delay Block (DB).

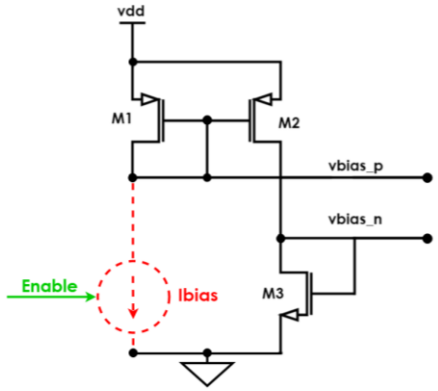

Figure 8. Bias generation circuit. In the simulations shown in section IV, is considered an ideal current source.

4 Simulations Results

The baseband logic in Fig. 2-A has been implemented in STMicroelectronics 90-nm BCD technology. The circuit is designed to interact with the clockless AFE described in [10] with a bit rate of 1 kbps. To have the period of the three stages ring oscillator equal to the bit time ($T_{ck} = T_b = 1$ ms) in nominal conditions, $I_{bias} = 2$ nA and $C = 1.1$ pF were chosen. In Fig. 9 the simulated waveforms corresponding to the operation of the circuit at room temperature are shown, indicating the correct behavior of the circuit.

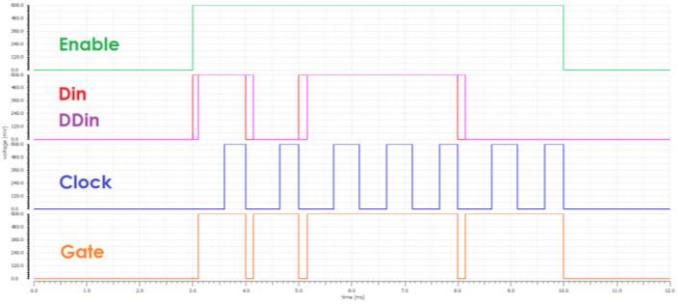

Fig. 9. Simulation results: Enable (green trace) triggers the GO that, starting from Din (red trace) first edge, generates the clock (Clock , blue trace). Clock samples DDin (violet trace) in the middle of the bit time, Gate (orange trace) resets Clock to 0 for any Din edge. In nominal conditions: $\tau_{d,rise} = 163$ µs, $\tau_{d,fall} = 146$ µs, $\tau_{d,res} = 340$ ns.

At room temperature $T_{ck} = 1$ ms, $\tau_{d,rise} = 163$ µs and $\tau_{d,fall} = 146$ µs showing that (1) is largely satisfied. Condition (2) is also verified since $\tau_{d,res}$ turns out to be 340 ns and therefore negligible compared to τ_d. The start-up delay of the oscillator τ_{resp} is defined as the absolute value of the difference between $T_b/2$ and the first low-high transition of the clock subsequent to a low-high transition of the Gate signal. In nominal conditions $\tau_{resp} = 7$ µs. Similarly, the settling time $\tau_{settling}$ of the oscillator is calculated as the difference between the first low-high transition time of the clock and the low-high transition time of the Enable signal. In nominal conditions $\tau_{settling} = 5$ µs. From the protocol point of view this means that no preamble is needed to settle the oscillator.

The impact of the CDR on the sensitivity of the receiver was evaluated performing transient noise simulations. The simulated clock rms jitter turns out to be lower than 1 µs, which is negligible with respect to the clock period. This allows to employ the proposed CDR without compromising the performances of the AFE.

A. Power consumption

During phase 1 (i.e. when Enable=0) the power consumption of CDR is due only to leakage currents and is $P_{ph1} = 0.162$ nW. During phase 2 the energy consumption is $E_B = 4.23$ pJ/bit resulting in a power consumption $P_{ph2} = 4.23$ nW at 1-kbps data rate. E_B and P_{ph2} are evaluated over a pseudo-random sequence of 100 bits. The contributions of the CDR blocks to P_{ph1} and E_B are depicted in Fig. 10 and 11, respectively. The CL contributions to P_{ph1} and E_B are 4.62 nW and 4.79 pJ/bit, respectively. Therefore, the baseband overall power consumption is 4.78 nW during the rest state and 9 pJ/bit at 1-kbps data rate.

B. Phase and frequency accuracy

Fig. 12 shows the clock frequency variation over temperature for $I_{bias} = 2$ nA. In the range -25 °C to +125 °C the frequency variation normalized to its nominal value is less than 10%. The frequency can be corrected by changing I_{bias} in the range 2.3 nA - 1.9 nA. The clock frequency varies from +6% to -10% when the supply voltage V_{dd} changes from 525 mV to 675 mV (+/- 12.5%). In order to restore $T_{ck} = T_b$ when $V_{dd} = 525$ mV I_{bias} should be reduced to 1.93 nA, while when $V_{dd} = 675$ mV it has to be increased to 2.35 nA. Simulations have been performed also with process corner parameters. In particular, in the worst cases, the frequency varies from -15% to +12%. In such cases I_{bias} value has to be changed from 2.4 nA to 1.8 nA in order to restore $T_{ck} = T_b$. In all simulated PVT conditions, the delay values satisfy the constraints given in section II.

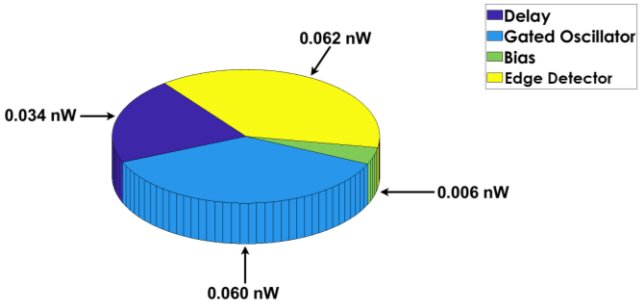

Fig. 10. Power consumption of the CDR during phase 1. CDR overall power consumption during phase 1 is $P_{ph1} = 0.162$ nW.

As discussed in paragraph II-B, $T_{ck} \neq T_b$ due to PVT variations induce a limitation in the NECB. For the above corner conditions, with fixed $I_{bias} = 2$ nA the NECB is limited to 2 bits. If a Manchester code is used this is not a problem, as verified through simulations. An alternative solution to the use of a Manchester code is trimming I_{bias} in order to compensate for the aforementioned f_{ck} variations by means of a calibration network like the one proposed in [8]. When the frequency error is reduced to 10% the NECB is equal to 3 bits and it is obtained in the worst case, while it increases to 35 with 1% of frequency accuracy.

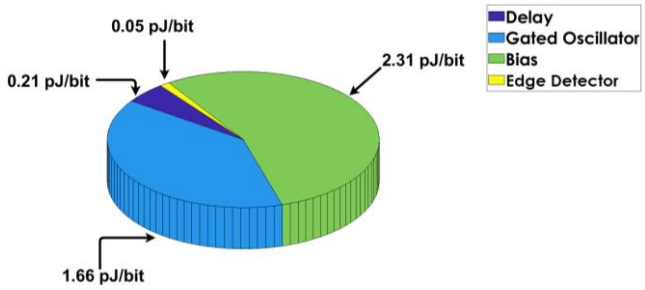

Fig. 11. Energy/bit consumption of the CDR during phase 2. At 1-kbps data rate the CDR overall power consumption is P_{ph2} =4.23 nW. CDR blocks contribution to P_{ph2} are: $P_{ph2,Delay}$ = 0.21 nW, $P_{ph2,Gated\ Oscillator}$ = 1.66 nW, $P_{ph2,Bias}$ = 2.31 nW and $P_{ph2,Edge\ Detector}$ = 0.05 nW.

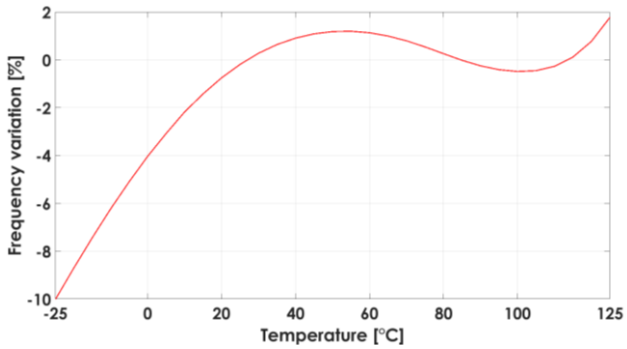

Fig. 12. Clock frequency variation with temperature.

5 Conclusion

This paper presents the design of a data-startable baseband logic allowing wake-up receivers (WuRx) to be employed in applications requiring the transmission of long sequences of bits. The proposed baseband logic includes a control logic with addressing capabilities and a clock and data recovery (CDR) block based on a Gated Oscillator (GO). It ensures phase alignment between received data and clock with high energy-efficiency, thus allowing to correctly sample infinite bits without power-hungry PLLs or crystal oscillators. The difference between the GO frequency and the data rate does not limit the maximum number of received bits, but only the maximum number of equal consecutive bits (NECB). Since the GO is started only upon reception of the first data edge, this solution is well suited for WuRxs based on a clockless analog front-end. The proposed solution is implemented in STMicroelectronics 90-nm BCD technology 1.2 V supply. To reduce overall power consumption, the baseband logic (CDR and control logic) has been supplied with 0.6 V. The CDR circuit consumes only 0.162 nW during the rest state and 4.23 pJ/bit at 1-kbps data rate. Simulations indicate that the maximum NECB, in the worst PVT case, is limited to 2. A Manchester code can be used to circumvent this problem. In alternative, the maximum NECB can be increased by reducing the frequency error (NECB = 35 bits with a 1% of frequency error), possibly by means of an additional calibration network.

References

[1] P. P. Mercier, A. P. Chandrakasan, “Ultra-Low Power Short-Range Radios”, Springer, 2015.

[2] J. Moody, P. Bassirian, A. Roy, N. Liu, S. Pancrazio, N. S. Barker, B. H. Calhoun, S. M. Bowers, “ A -76dBm 7.4 nW Wake-Up Radiowith Automatic Offset Compensation”, ISSCC, pp. 452-453, Feb. 2018.

[3] P. H. P. Wang, H. Jiang, L. Gao, P. Sen, Y. H. Kim, G. M. Rebeiz, P. P. Mercier, D. A. Hall, “ A Near-Zero-Power Wake-Up Receiver Achieving -69-dBm Sensitivity”, IEEE Journal of Solid State Circuits, Vol. 53, No. 6, June 2018.

[4] S. Oh, N. E. Roberts, D. D. Wentzloff, “A 116 nW Multi-Band Wake-Up Receiver Achieving -69-dBm Sensitivity“, Proceedings of the IEEE 2013 Custom Integrated Circuits Conference, 2013.

[5] V. Mangal, P. R. Kinget, “A 0.42 nW 434 MHz -79.1 dBm Wake-Up Receiver with a Time Domain Integrator”, ISSCC, pp. 438-439, Feb. 2019.

[6] M. Elhebeary, L. Y. Chen, S. Pamarti, C. K. K. Yang, “An 8.5 pj/bit Ultra-Low Power Wake-Up Receiver Using Schottky Diodes for IoT Applications”, ESSCIRC, pp. 205-208, Sep. 2019.

[7] https://www.iis.fraunhofer.de/en/ff/sse/icd/leist/asic/wakeup.html.

[8] M. Hsieh, G. E. Sobelman, “Architectures for Multi-Gigabit Wire-Linked Clock and Data Recovery”, IEEE Circuits and Systems Magazine, Fourth Quarter 2008.

[9] J. S. The, R. P. Arjun, L. Siek, Y. Zheng, “Review of Pulse Generators for Gated Ring Oscillator Based Time-to-Digital Converters”, International Symposium of Integrated Circuits, 2016.

[10] A. Elgani, M. Magno, F. Renzini, L. Perilli, E. Franchi Scarselli, A. Gnudi, R. Canegallo, G. Ricotti, L. Benini, “Nanowatt Wake-Up Radios: Discrete-Components and Integrated Architectures”, 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2018.

[11] M. Elhoseny and A. E. Hassanien, "Secure Data Transmission in WSN: An overview", Dynamic Wireless Sensor Networks, pp. 115-143, Springer, 2019.

[12] T. Wada, M. Ikebe and E. Sano, “60-GHz, 9-µW Wake-up Receiver for Short-Range Wireless Communications”, ESSCIRC, pp. 383-386, Sep. 2013.

[13] K. W. Cheng, J. S. Lin, S. E. Chen, “Reference-Less Ultra-Low-Power Wake-Up Receiver with Noise Suppression”, URSI Asia-Pacific Radio Science Conference, pp. 994-997, Aug. 2016.